Nonlinear analysis of a microwave fractional synthesizer

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Abstract — **In this work, the nonlinear analysis of a fractional phase-locked loop with 2.4 GHz output frequency is presented. The nonlinear simulation uses a realistic description for the phase-frequency detector and the loop filter. The phase-error compensation for beat-note spurious reduction is analyzed, predicting the attenuation values for practical and theoretically improved compensation signals. The influence of different loop parameters on the beat note spurious is also studied, through the application of the Poincaré map. This technique has also enabled the determination of the phase-locked ranges, delimited by chaotic phenomena. The phase-locked loop has been manufactured and experimentally characterized.**

I. Introduction

In a fractional synthesizer [1-4], the output frequency is a fractional multiple of the reference frequency, i. e., $f_{VCO}=f_r(N+K/F)$, with K<F. The narrow channel spacing is given by $\Delta f=f_r/F$, so the reference frequency can be F times higher than in a conventional integer synthesizer. This enables a wider loop-filter bandwidth and, thus, fast switching times. The decrease of the division ratio also reduces the output phase-noise. The overflow of an accumulator [1-3] is used to periodically vary the division order between N and N+1. This instantaneous modulation of the division ratio creates spurious tones at f_r/F (beat note) in the output spectrum. The beat note can, however, be corrected through phase-interpolation, using a digital-to-analog converter. The contents of the accumulator are used to create a compensation signal, which is summed into the loop filter. Other approaches for beat note reduction include the use of sigma-delta modulators [4].

In the bibliography, several works have been devoted to the study and design of fractional synthesizers, using an phase interpolation. In [1] analytical expressions are obtained for the phase error and for the spurious tones, after introduction of the compensation signal. In [2], a nonlinear simulation is presented, using normalized units. The aim here is to carry out a realistic analysis of the synthesizer global behavior, with accurate models of the digital phase detector and the loop filter. The optimum compensation signal will be mathematically determined and compared with existing techniques. The influence of different loop parameters on the spurious content, phase-locked ranges and settling times (when the channel is switched) will be studied.

II. NONLINEAR ANALYSIS OF THE FRACTIONAL PHASE-LOCKED LOOP

The fractional PLL analyzed here has 2.4 GHz output frequency. The frequency range of the voltage-controlled oscillator (VCO) is 2-3 GHz. For the nonlinear simulation, the truth table of the digital phase detector (PD) is taken into account. For the analysis, the fractional modulus F=5 will be considered.

A Phase error and compensation current

For a fractional PLL with division ratio N+K/F, there are K divisions by N+1 and F-K divisions by N in F cycles of the reference signal. The division order can be modulated using the output of an F-modulus accumulator. The accumulator changes its value $a_c(n)$ (with n = 1 to F) at each cycle of the reference $T_r=1/f_r$, returning to its initial value after F cycles, i.e., with the period F/f_r. The instantaneous variation of the division order (N or N+1) gives rise, at the phase-detector input, to a phase error $\phi(n)$, whose value depends on the accumulator content $a_c(n)$.

When the division order is not modulated (integer divider), the phase-locked solution of the PLL is given by a constant phase error ϕ_o at the phase-detector input. For a filter pole located at the origin, this phase error will either be $\phi_o = 0$ or $\phi_o = \pi$, the actual value depending on the loop parameters. If no filter poles are located at the origin, the phase error ϕ_o will be different from these two values [5]. In fractional PLL this value is shifted by fractional averaging and modulated by the beat note. Then the phase error can be expressed:

$$\phi(t) = \phi_{oB} + \phi_B(t) \qquad (1)$$

where ϕ_{oB} and $\phi_B(t)$ are defined such that $\phi_{oB}, \phi_B(t) < 0\ \forall t$ and $\phi_{oB} \geq \phi_B(t)\ \forall t$. A negative phase error has been assumed. The analysis for positive error can be carried out in similar way. The time variation $\phi_B(t)$ is responsible for the beat-note modulation. The width of each pulse at the PD output is determined by the phase-error value at its falling edge.

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In Fig. 1a, the input signals to the phase detector $v_r(t)$ and $v_o'(t)$ have been represented, respectively corresponding to the reference signal and the output of the frequency divider, together with the PD output pulse, all in normalized units to enable the comparison. As shown in Fig. 1a, the pulse width at each reference period is $1/f_r$-$\Delta t(n)$, with:

$$\Delta t(n) = -\frac{\phi\left(\frac{n}{f_r} - \Delta t(n)\right)}{2\pi f_r} = -\frac{\phi_{oB}}{2\pi f_r} - \frac{\phi_B\left(\frac{n}{f_r} - \Delta t(n)\right)}{2\pi f_r} \quad (2)$$

The second term of (2) repeats its value each M reference cycles and is thus responsible of the beat note (see Fig. 1b). In other works [1], $\Delta t(n)$ has been calculated neglecting ϕ_{oB}. As gathered from (2), this gives rise to an error in the estimation of $\Delta t(n)$. Taking (2) into account, the expression in [1], relating the beat note $\phi_B[n/f_r-\Delta t(n)]$ to the accumulator content $a_c(n)$, is modified to:

$$\phi_B\left(\frac{n}{f_r} - \Delta t(n)\right) = -2\pi\frac{a_c(n)}{(NF+K)} - 2\pi\frac{K - M\,x_N(n)}{(NF+K)}\frac{\phi_{oB}}{f_r} \quad (3)$$

where $x_N(n)$ is equal to 1 for instantaneous division order N+1 and equal to zero for instantaneous order N. As shown in (3), the beat note decreases with N.

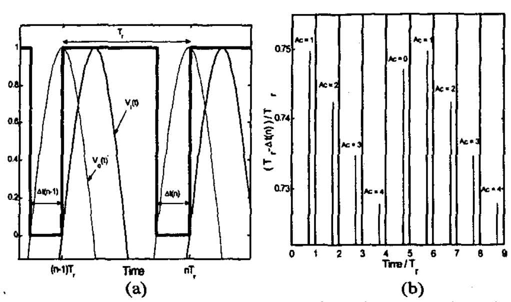

Fig. 1 Phase error for K/F=1/5. (a) Voltage input signals to the PD and PD output current pulse. All signals are normalized for the comparison. (b) Phase error-pulse sequence over two beat-note periods (2F).

The error current is responsible for a charge injection, given by the integral of the current error pulses [1]. The modulation of this area determines the amplitude of the beat note frequency in the output spectrum. The beat note is generally compensated through the injection, into the loop filter, of a pulsed current $i_c(t)$ of constant pulse width and variable height, having the same area modulation as (3) and period F/f_r. The signal at the output of the prescaler generally employed in the implementation of the frequency divider can be used in the generation of the compensation signal. For a prescaler of order P, the width of the compensation-current pulses will be: f_{VCO}/P, with f_{VCO} being the frequency of the voltage-controlled oscillator (VCO).

In practical realizations of the compensation signal, the amplitude of $i_c(t)$ is empirically fitted, this meaning a multiplication of $i_c(t)$ by an adjustable factor η, i.e., $i_c'(t)=\eta i_c(t)$. Actually, the optimum phase-error compensation would be the one provided by a current signal having equal amplitude and opposite phase at the beat note frequency f_r/F. Taking this into account, the influence of both the pulse amplitude and width has been studied here. The constant pulse width is written $\tau=\gamma P/f_{VCO}$, with γ, a variable parameter.

The nonlinear simulation carried out here enables the prediction of the beat note attenuation. Fig. 2 shows the improvement in the beat-note attenuation when the compensation current is calculated from the phase-error model (3), compared to the model neglecting ϕ_{oB}. The improvement due to the fitting of the pulse width only has an appreciable influence for relatively low division order N. The maximum attenuation of the beat note is obtained for η close to unity $\eta\cong 1$, but not exactly unity, in agreement with the experimental observations.

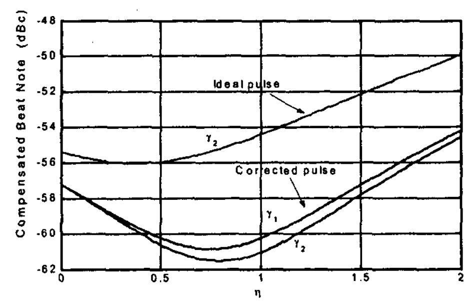

Fig. 2 Attenuation of beat-note frequency. The parameter η indicates variations of the pulse amplitude with respect to ideal area compensation (η=1) and γ, variations in the pulse width with respect to $\tau=P/T_{VCO}$ (γ=1).

Fig. 3a and Fig. 3b respectively show the synthesizer experimental spectrum before and after compensation, for γ=1. The spectrum has been measured at the output of the VCO. Fig. 3c shows the spectrum simulation, before and after compensation, in the same conditions. Note that, since F=5, there are three other spurious tones $kf_r/5$, with k=2,3,4, between the beat note and the reference line at f_r.

B Parameter influence on the behavior of the fractional synthesizer

a) Beat note

The influence of the loop-filter bandwidth ω_B on the beat note value has been analyzed. It is a typical second-order RC filter, whose response can be modeled with the equation: $F(s)=(s+\tau_1)/[(s+\tau_2)(s+\varepsilon)]$. One of the filter poles is ideally located at the origin $\varepsilon=0$. However, parasitics in the capacitors and the finite output impedance of the charge pump give rise to a slight shift. Here the analysis parameter is the filter bandwidth ω_B, with a relatively low division order N (for an easier visual appreciation of the qualitative effects). The analysis is carried out through the use of the Poincaré map [7]. This map is obtained by sampling the steady-state solution at integer multiples of the reference period T_r. The resulting discrete points are represented versus the parameter ω_B (Fig. 4).

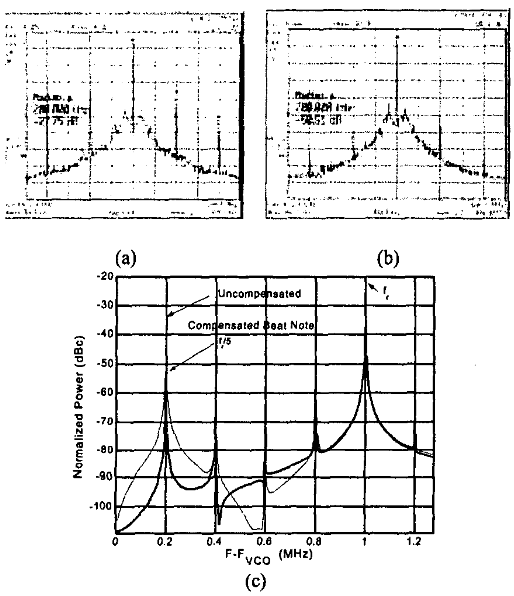

Fig. 3 Compensation of beat-note frequency. (a) Experimental, before compensation. (b) Experimental, after compensation. (c) Simulation of both cases. Other spurious lines and the reference frequency f_r are also shown.

In fractional synthesizers, for phase-locked operation, the sampling provides F different points. Out of lock, the sampling provides an ensemble of points, corresponding to either quasi-periodic or chaotic behavior. In the ω_B interval of phase-locked behavior, the width of the vertical line, defined by the F points, enables a visual estimation of the beat note. The beat note is smaller for smaller amplitude of the Poincaré section (given by the F points).

This is shown in Fig. 4, where the two cases of compensated and uncompensated beat note have been considered. In each case, five discrete points are obtained in the interval of phase-locked behavior, due to the fractional value F=5. For compensated beat note, the five points are closer together. Due to the natural decrease of the beat note with the division order N (see (3)), a relatively low N has been considered for this analysis is order, to enable a better appreciation of the influence of bandwidth ω_B. The beat-note amplitude decreases with ω_B in case of an uncompensated signal. Actually, the larger bandwidth implies a less selective filter and thus less attenuation of the beat note. For an uncompensated signal, the beat-note amplitude keeps approximately constant. As shown in Fig. 4, for the N value considered in the simulation, the loop unlocks, for very narrow bandwidth. This is due, as will be shown in the next paragraph, to the onset of chaotic solutions. The value of the filter bandwidth $\omega_B \cong 80$KHz, for the onset of chaos is approximately the same in the two cases of compensated and uncompensated signal.

Another parameter with high influence on the beat note magnitude is the division order N. The beat note increases for small division order N. This can be understood due to the higher relative influence of the division-order modulation for smaller N values. The next analysis of phase-locked ranges versus N will illustrate this point.

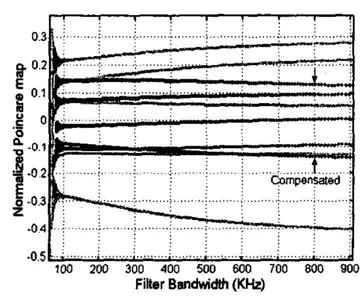

Fig. 4 Poincaré map. Influence of the filter bandwidth ω_B on the beat-note amplitude.

b) Phase-locked ranges

In preliminary simulations of the fractional synthesizer used here, it has been found that its *hold-in* and *lock-in* ranges are beyond the maximum operation frequency of the synthesizer. Instead, unlocked behavior has been experimentally observed (see Fig. 5) inside the region for which phase-locked operation region is usually expected (output frequency close to that of the free-running oscillator and high loop gain). These unlocked solutions are, in fact, chaotic solutions. The fractional division probably makes the observation of these solutions more likely, due to the introduction of the beat note frequency. The beat note is an F-order subharmonic of the reference frequency, which makes the nonlinear dynamics of the loop more complex. The phase-locked ranges are easily determined through the use of the Poincaré map. This has been done in Fig. 6, where the two cases of a fractional loop with and without compensation can be compared. As can be seen, there is an increase of the beat-note amplitude as N decreases. Again, the onset of chaos takes place for approximately the same N value in the two cases of compensated and uncompensated beat note.

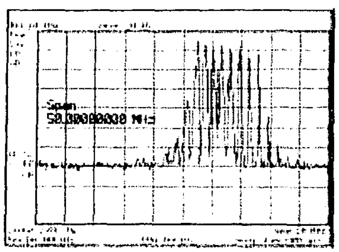

Fig. 5. Experimental unlocked spectrum observed for the loop parameters: N=2043, f_r=1 MHz, K/F=2/5. It corresponds to a chaotic solution.

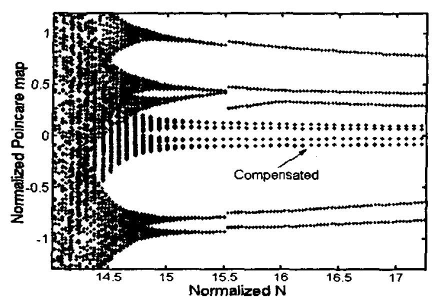

Fig. 6 Poincaré map versus the division order N

c) Settling time

The settling time when switching the channel from f_{VCO}=(N+1/F)f_r to f'_{VCO}=(N+4/F)f_r has also been analyzed (Fig. 7), obtaining the value τ≅100μS. The simulation has been repeated for other value of fractional division F=8 and similar frequency variation Δf_{VCO}, obtaining a similar settling time. This time depends on the loop bandwidth and the absolute value of the frequency increment.

III. CONCLUSIONS

In this work the nonlinear analysis of a fractional phase-locked loop has been presented. The analysis enables the prediction of the beat-note amplitude in the output spectrum. A study of the optimum beat-note compensation signal has also been carried out and compared with standard compensation techniques. The Poincaré map is proposed as a simple technique to determine the influence on the beat note magnitude of different loop parameters. Unlocked solutions, commonly observed in the experiment for loop output frequencies close to that of the free-running oscillator, have been analyzed. The phase-locked ranges, delimited by these solutions, have been determined. The synthesizer has been manufactured and experimentally characterized, obtaining very good agreement with the simulations.

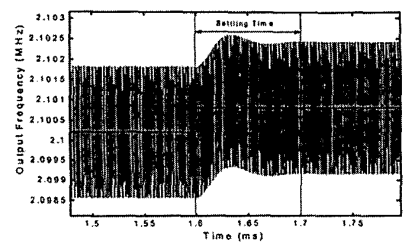

Fig.7 Simulation of settling time for channel switch from K=1 to K=4.

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